

1/16

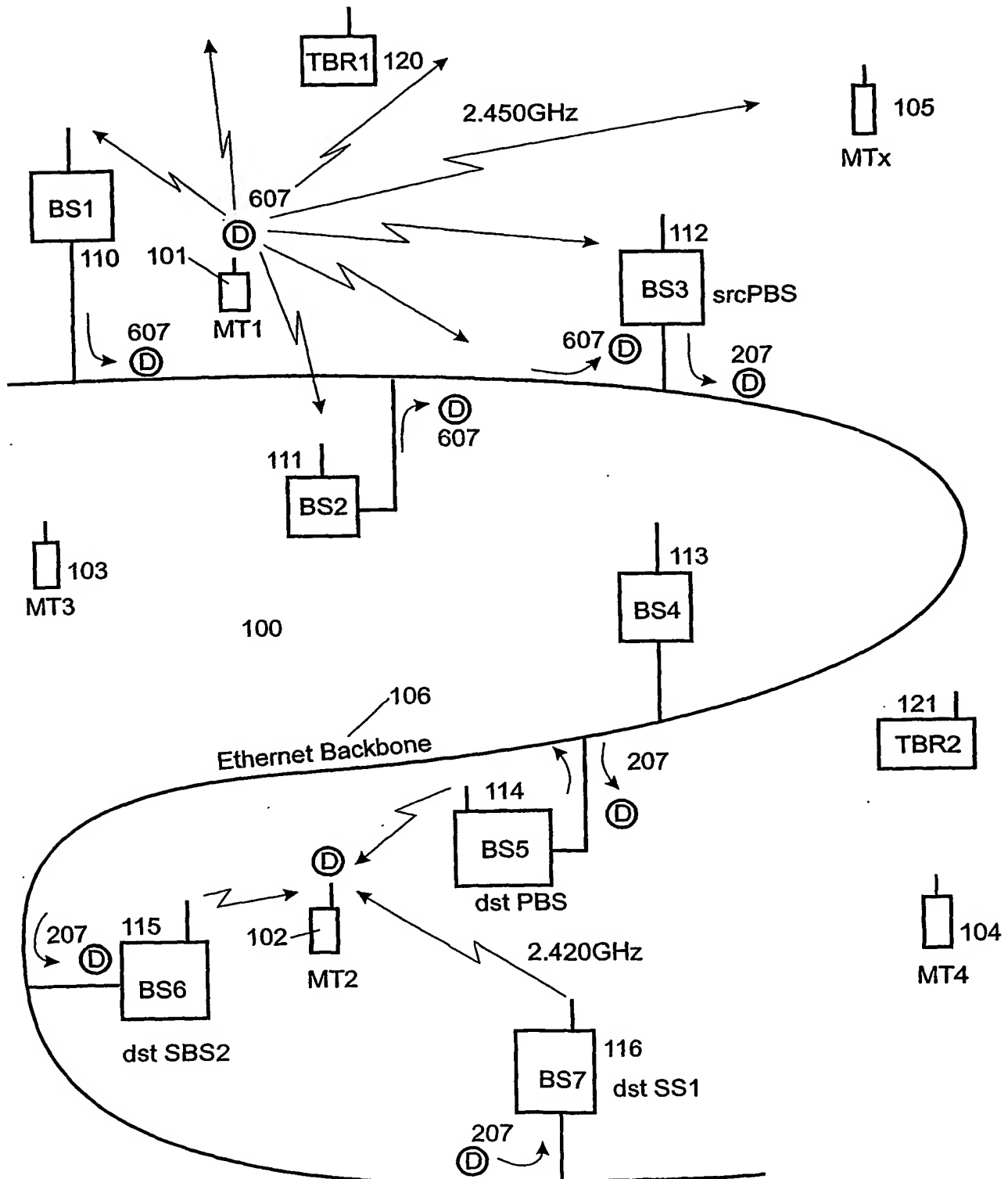


FIGURE 1

2/16

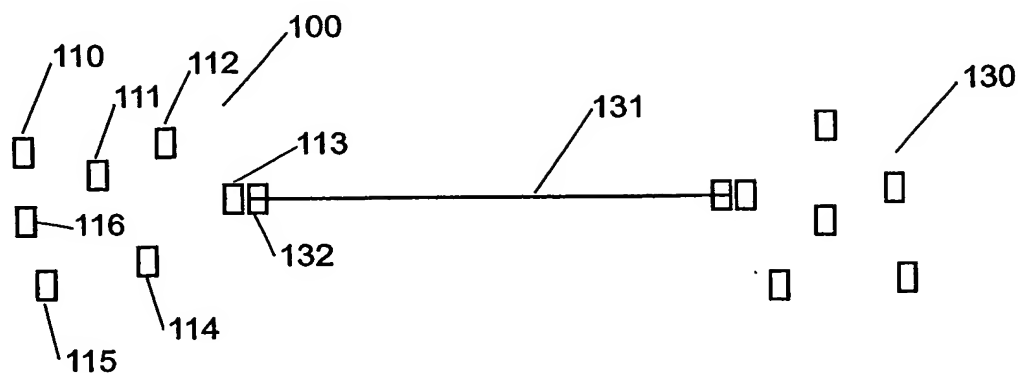


FIGURE 2

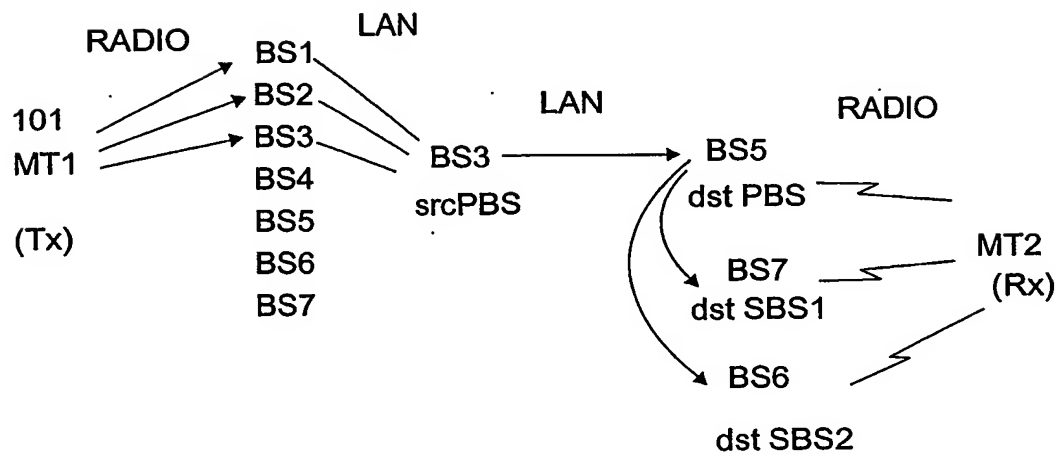


FIGURE 3

3/16

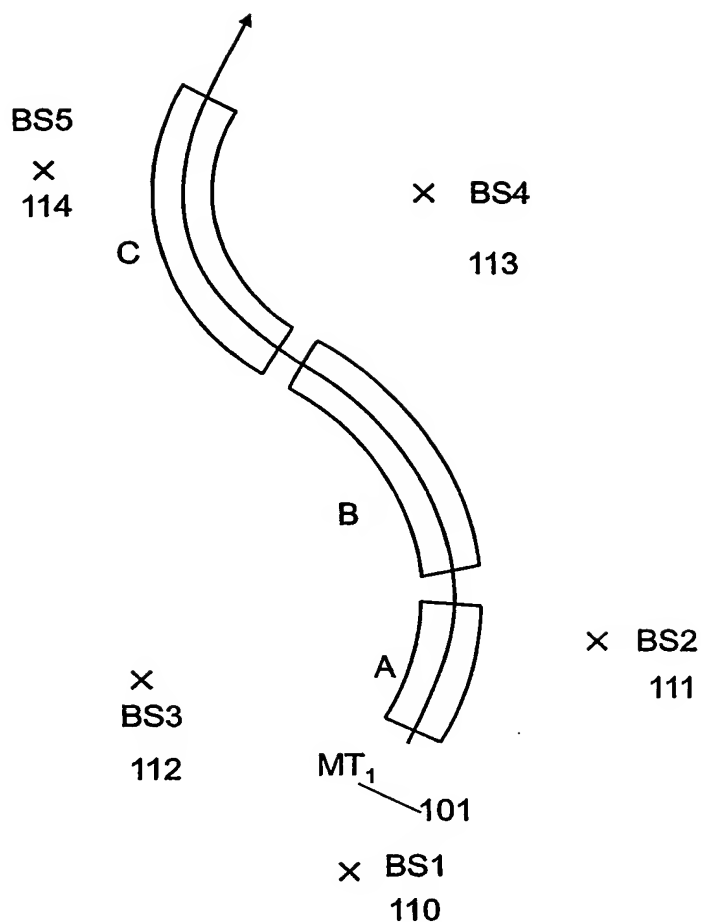


FIGURE 4a

	Src PBS	dst PBS	dst PBS ₁	dst PBS ₂
A	BS1	BS1	BS2	BS3
B	BS2	BS4	BS2	BS3
C	BS4	BS3	BS4	BS5

FIGURE 4b

4/16

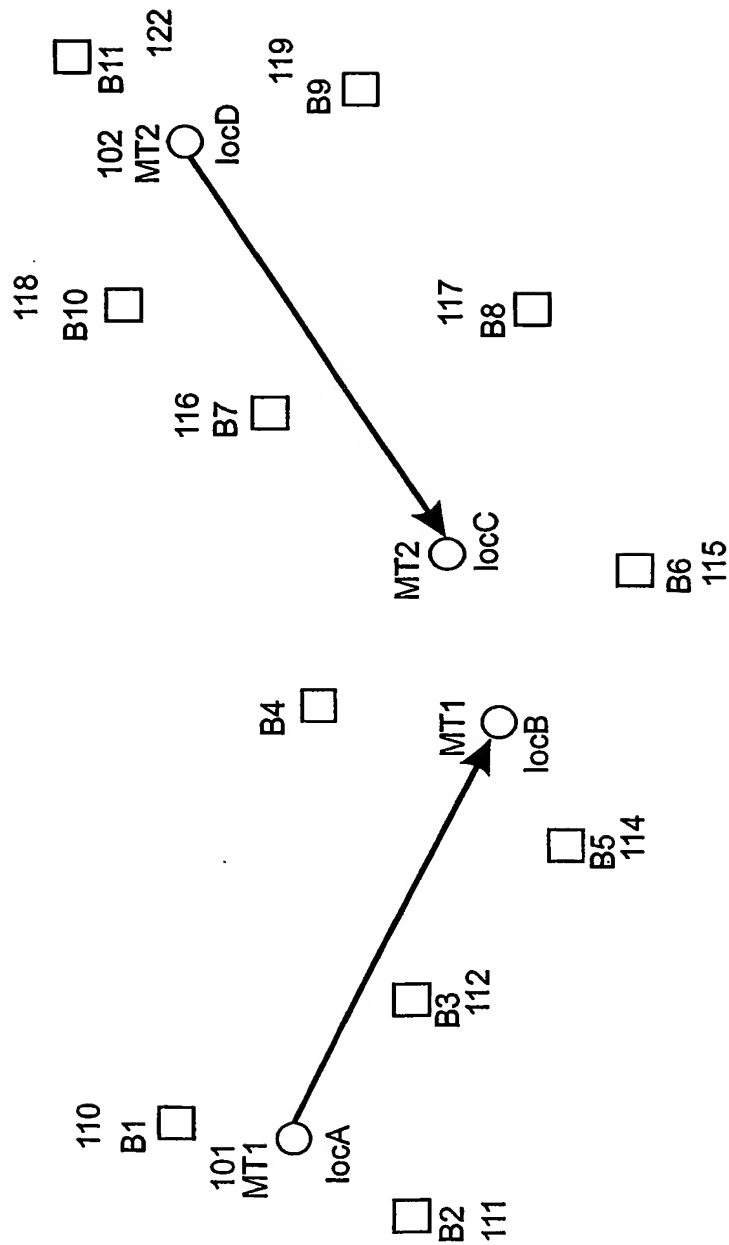


FIGURE 5

5/16

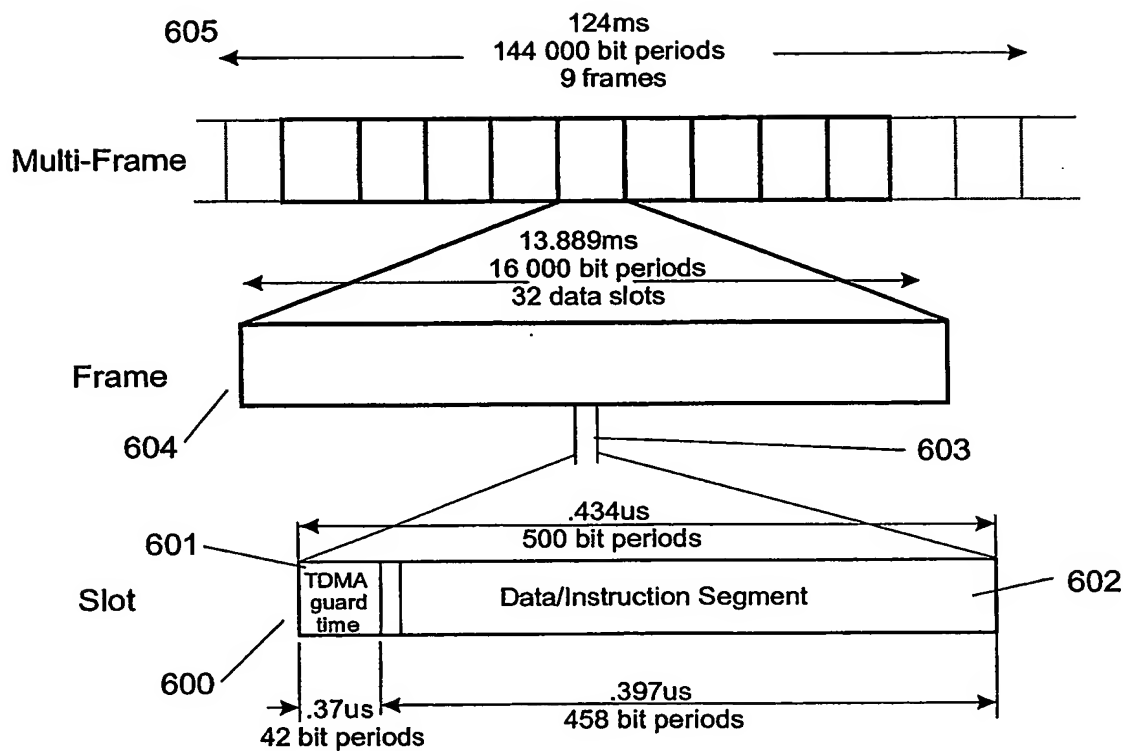


FIGURE 6a

6/16

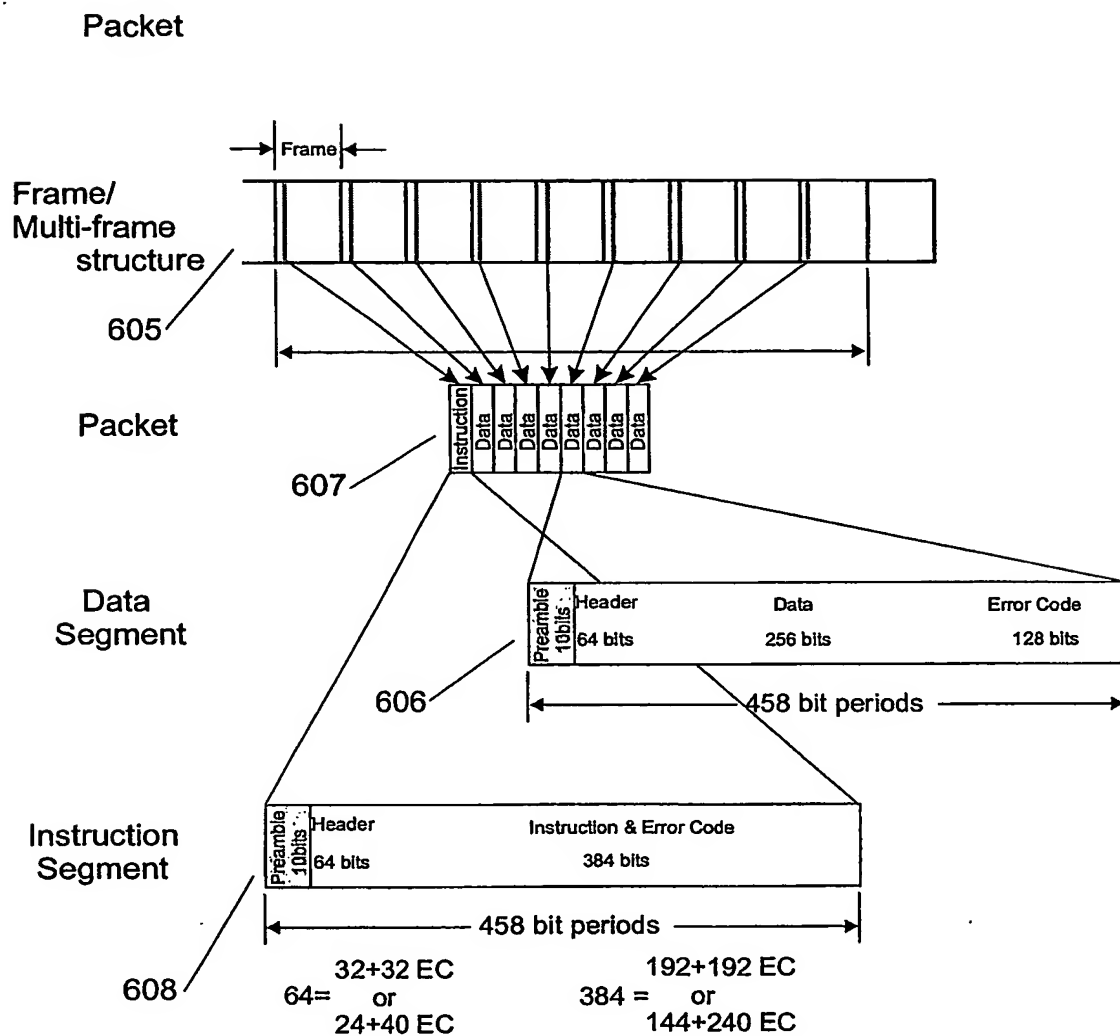


FIGURE 6b

7/16

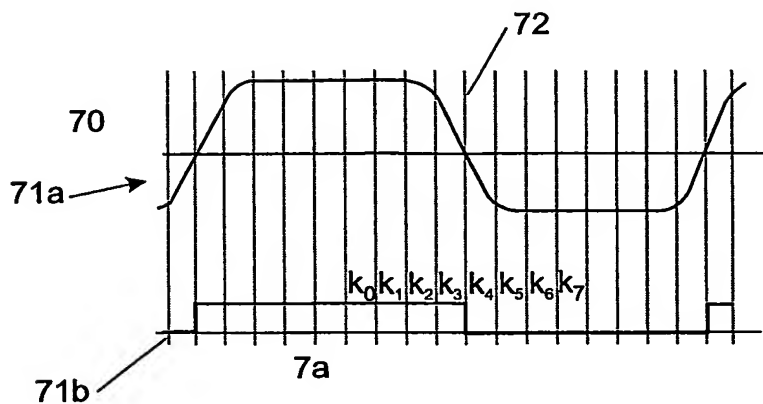


FIGURE 7a

Truth Table

k_0	k_1	k_2	k_3	k_4	k_5	k_6	k_7	x_n
x	1	1	1	0	0	0	x	1
x	1	1	0	1	0	0	x	1
x	0	0	0	1	1	1	x	1
x	0	0	1	0	1	1	x	1
x	ELSE						x	0

FIGURE 7b

'X' Don't Care

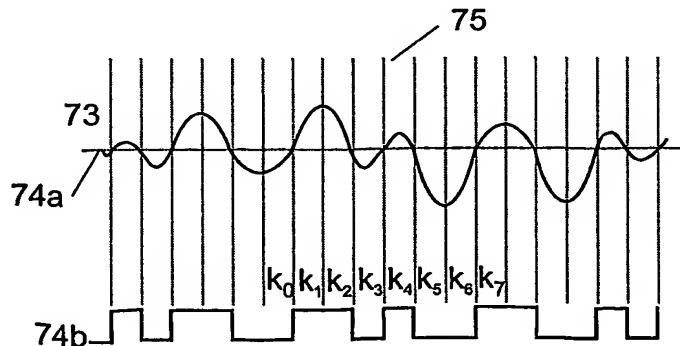
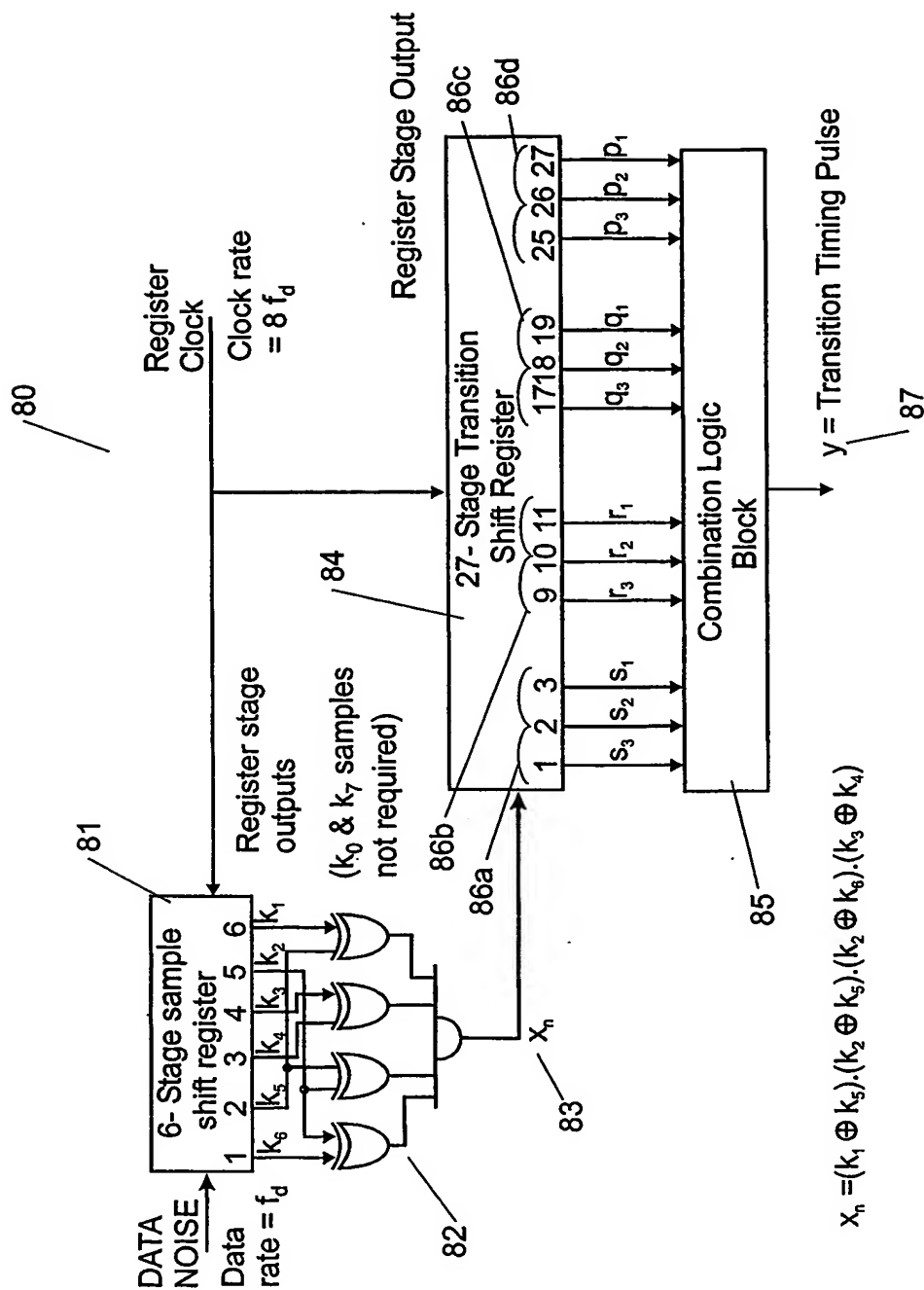


FIGURE 7c



Fast Symbol Timing System Block Diagram

FIGURE 8

9/16

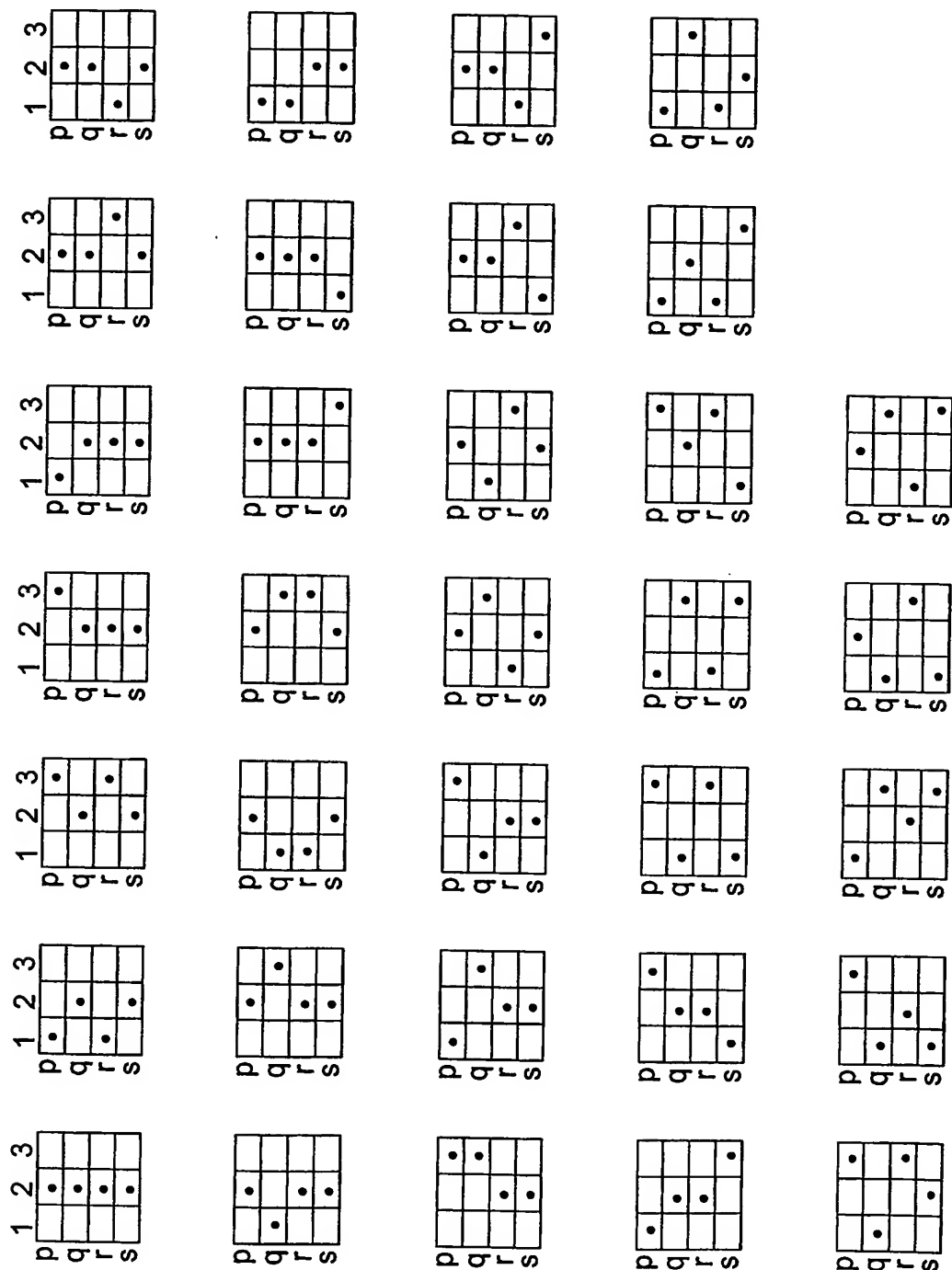


FIGURE 9a

10/16

$$\begin{aligned}
 y = & (q_2 s_2) (p_1 r_1 + p_2 r_2 + p_3 r_3 + p_2 r_1 + p_2 r_3) \\
 & + (q_1 s_2) (p_2 r_1 + p_1 r_2 + p_3 r_2 + p_2 r_3 + p_2 r_2 + p_3 r_3) \\
 & + (q_3 s_2) (p_2 r_2 + p_2 r_3 + p_3 r_2 + p_1 r_2 + p_2 r_1 + p_1 r_1) \\
 & + (q_2 s_3) (p_2 r_2 + p_2 r_1 + p_1 r_2 + p_1 r_1) \\
 & + (q_2 s_1) (p_2 r_2 + p_2 r_3 + p_3 r_2 + p_3 r_3) \\
 & + (q_1 s_1) (p_3 r_3 + p_3 r_2 + p_2 r_3) \\
 & + (q_3 s_3) (p_1 r_1 + p_1 r_2 + p_2 r_1)
 \end{aligned}$$

FIGURE 9b

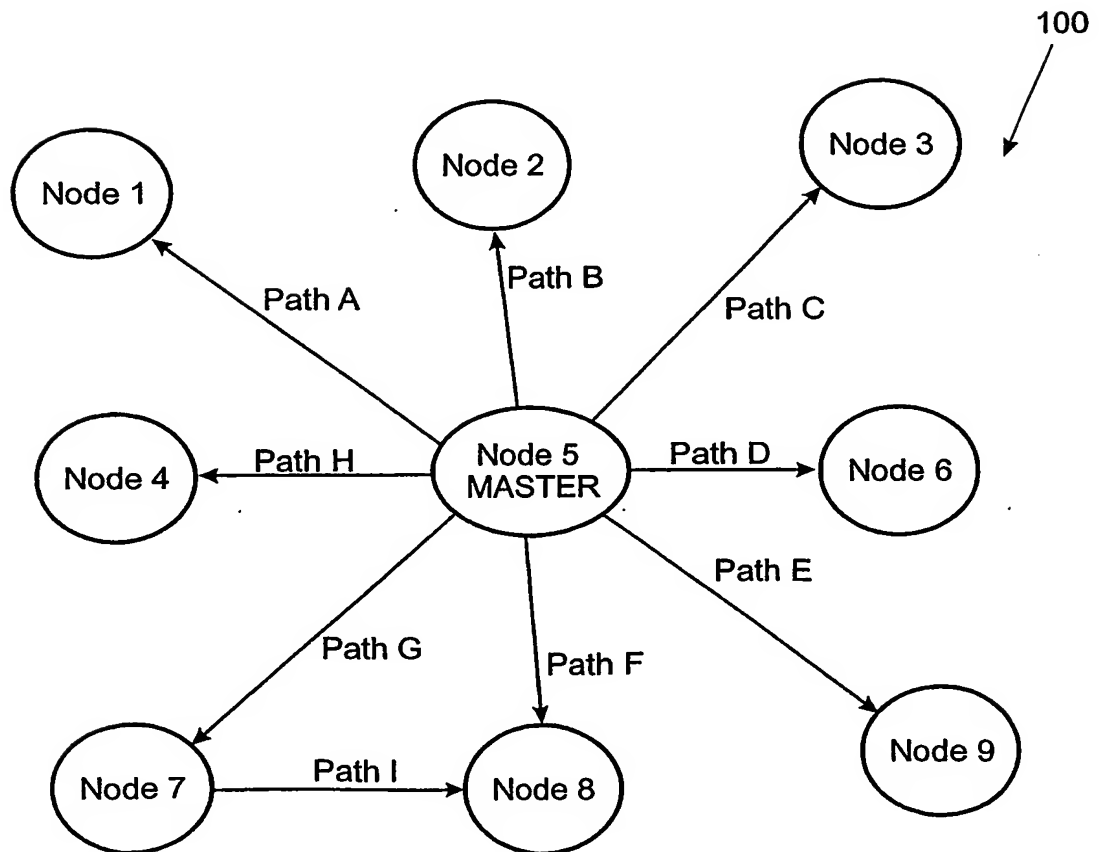


FIGURE 10a

11/16

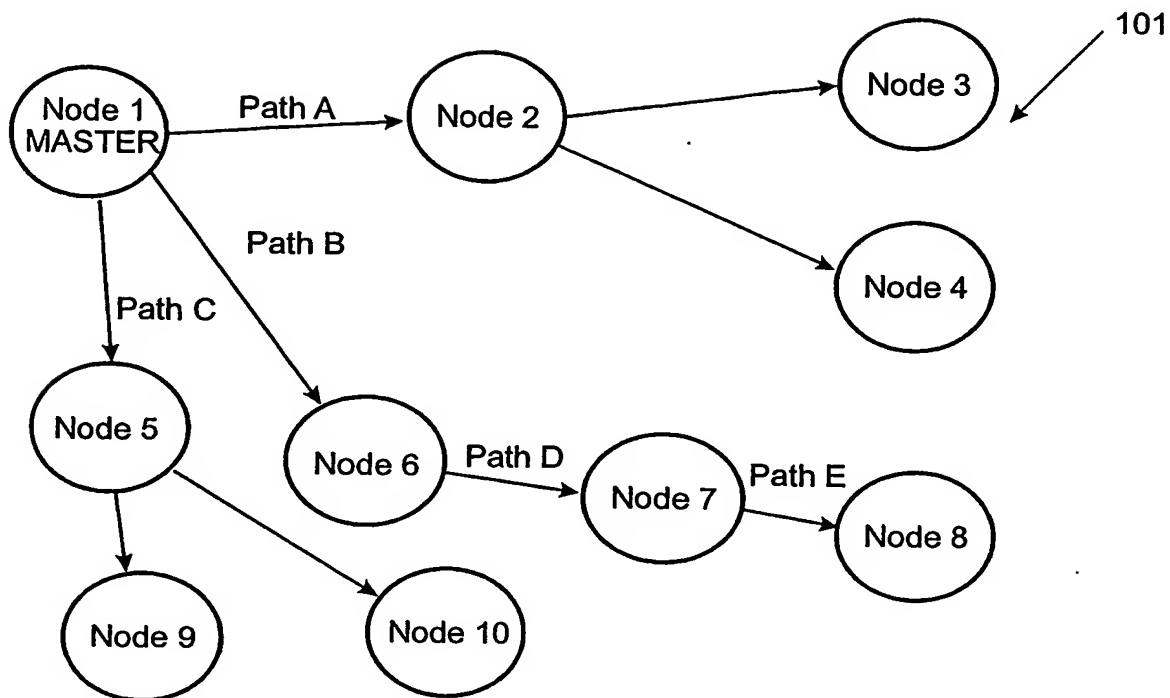


FIGURE 10b

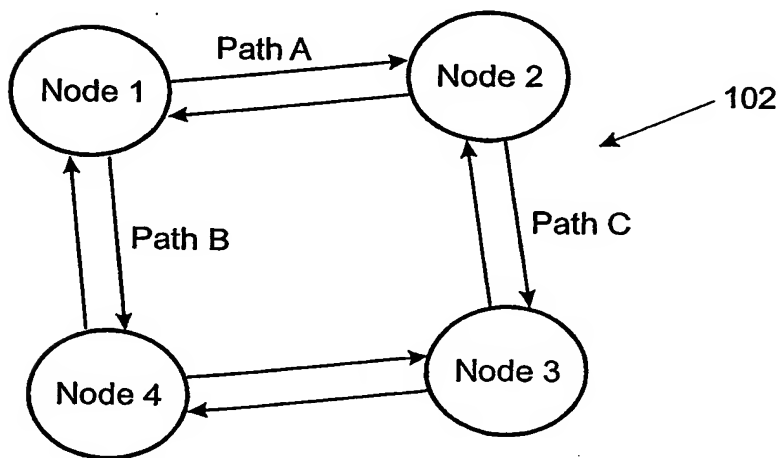


FIGURE 10c

12/16

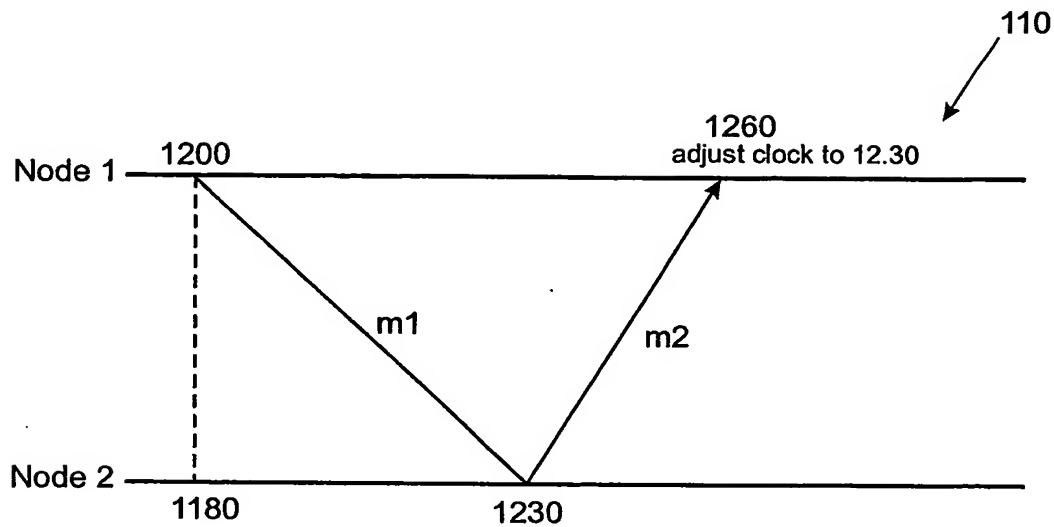


FIGURE 11a

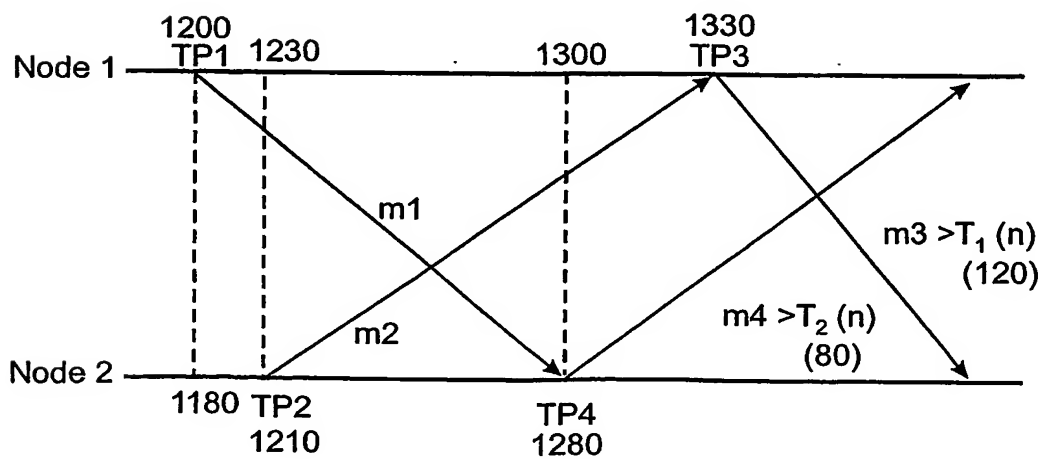


FIGURE 11b

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
120 sync word	0	0	0	0	0	1	0	1	1	0	0	1	1	1
121 HD=1	0	0	0	0	0	1	0	1	1	0	0	0	1	1
122	0	0	1	0	0	1	1	1	1	0	0	0	1	1
123 HD=0	0	0	1	0	0	1	1	1	1	0	0	0	1	1
124 HD=3	0	0	0	0	0	1	1	1	1	0	0	0	1	1

FIGURE 12

14/16

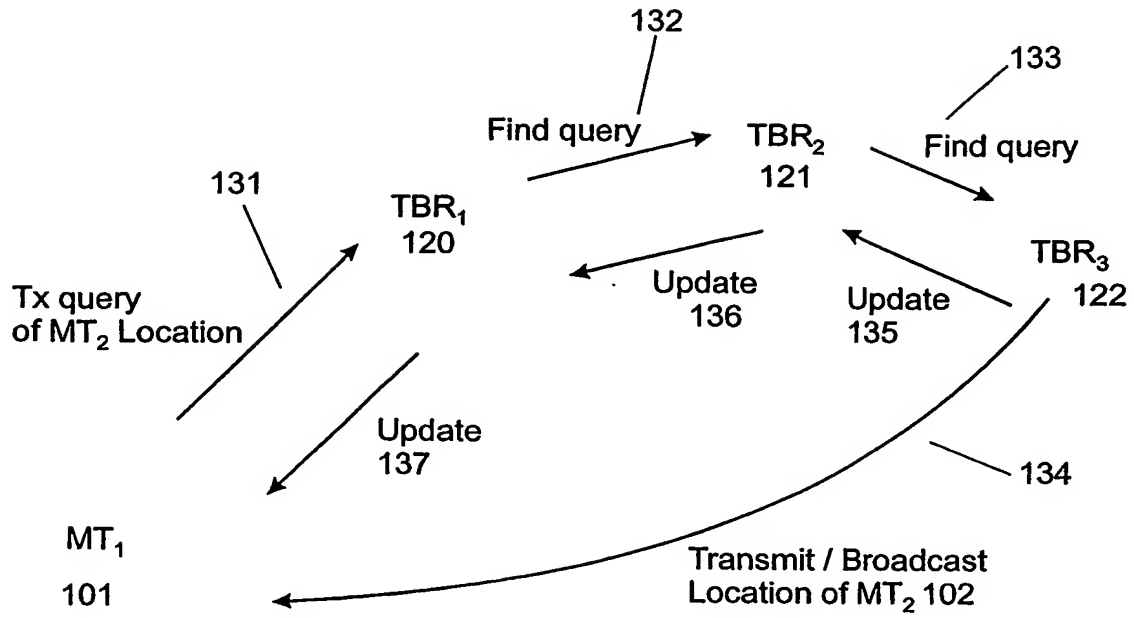


FIGURE 13

15/16

TERMINAL BASE REGISTER				
	Src PBS	Dst PBS	Dst SBS1	Dst SBS2
MT ₁	BS3 (1)	BS1 (3)	BS2 (4)	BS7 (5)
MT ₂	BS4 (20)	BS5 (32)	BS6 (31)	BS7 (19)
MT ₃	BS6 (19)	BS6 (22)	BS1 (13)	BS2 (4)
MT _x	BS3 (19)	BS4 (25)	BS3 (30)	BS1 (27)

FIGURE 14

16/16

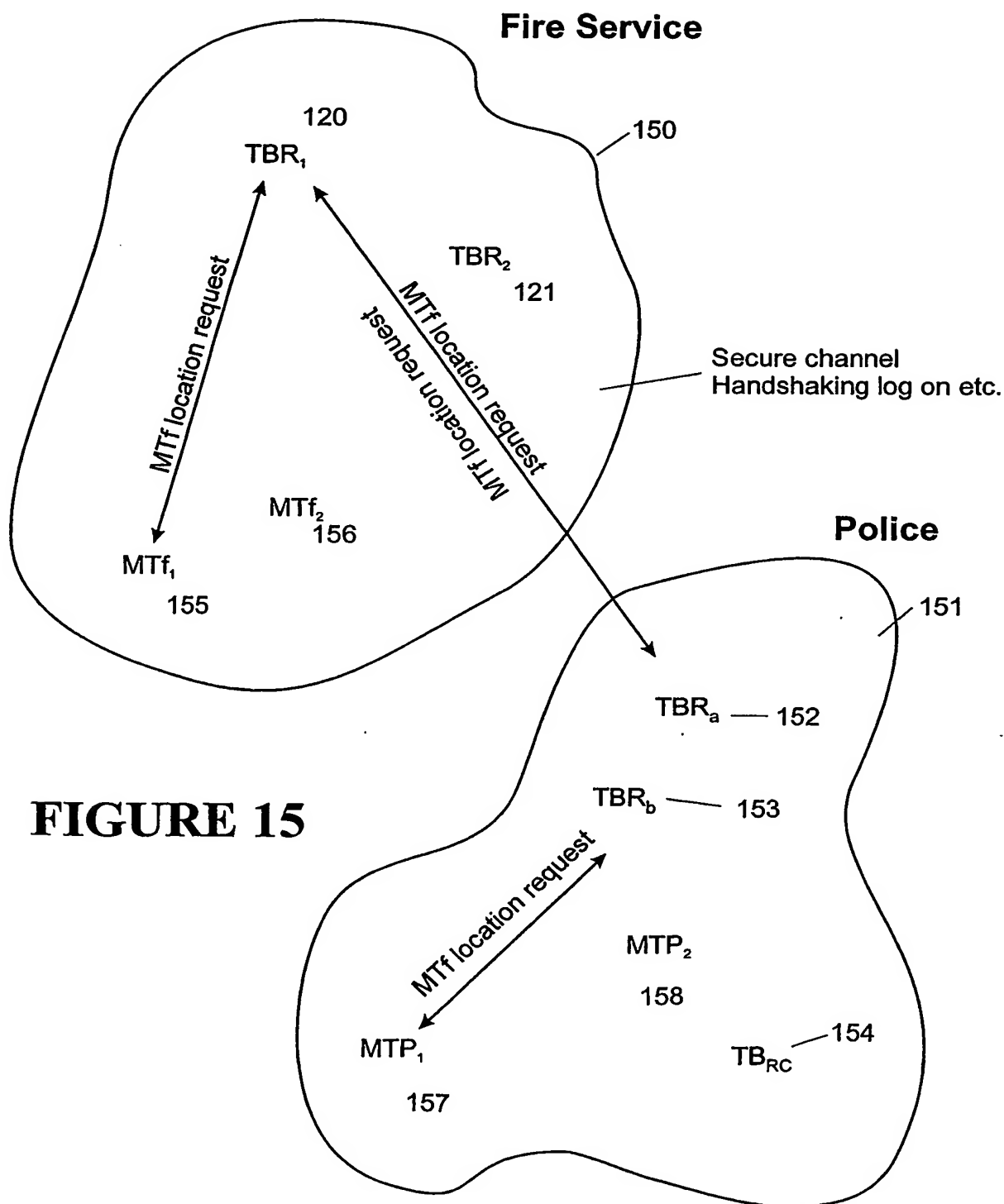


FIGURE 15